The Terminology of CS-322

Absolute v. Relative Branches Access Link / Static Link Activation Records (i.e., Stack Frames) Activation Tree Array Indexing Computations **Available Expressions** Available Expressions **Basic Block Big** / Little Endian Calling Sequence / Return Sequence Code Generation Algorithm #1 Code Generation Algorithm #2 **Common Sub-expression Elimination Constant Folding** Control Flow Graph (Initial Block, Predecessors, Successors) Control Link / Dynamic Link Control Stack (Frame Stack, Activation Record Stack) Copy Propagation DAG / Tree / Nodes / Edges / Root / Leaves / Interior Nodes **DAG-Based** Optimization Dangling Reference Dead Code (unreachable v. unnecessary) Definition-Use (D-U) Chains Direct Jump Table (as implementation of Switch Stmt) **Display Registers** Dominates Relation / Dominator Tree Dynamic Programming (approach to tiling) Global v. Local Approaches Graph Coloring Algorithm, K-Coloring Heap Heap Fragmentation Heuristic Algorithm Induction Variables Inherited v. Synthesized Attributes **Inline** Expansion Inner / Outer Loops Instruction Cost Models Instruction Scheduling Instruction Selection Interference Graph Intermediate Representation (IR)

Invocation **IR** Code Generation Leaders (of Basic Blocks) Lexical / Dynamic Scoping Lexical / Static Nesting Lexical Analysis / Regular Expressions Live / Dead Variable Live Variable Analysis Local / Non-local variables Loop Back Edges Loop Invariant Computations Loop Unrolling L-Value / R-Value Mapping Natural v. Unnatural Loops Next-Use Offset (into an activation record) **Optimization Phase of Compiler** Order Restrictions (in DAG-Based Optimization) Parameters (i.e., Formals) v. Arguments Parsing / Syntax Partial Order Pass By Name Pass By Reference Pass By Value Pass By Value-Result (i.e., Pass By Copy-Restore) Peephole Optimizer Physical Registers, Virtual Registers Point, Path (in Control Flow Graph) Preheader Quicksort Algorithm **Reaching Definitions Recurrence** Equations **Recycling Temporaries** Reducible Flow Graph Reduction in Strength **Register Allocation Register Allocation Strategies Register** Assignment Register Transfer Language (RTL) Register-to-Register Model (v. Memory-to-Memory Model) RISC Routine / Function / Procedure Row-Major Order / Column-Major Order Short-Circuit Evaluation SPARC: Alignment (word / double / quad)

SPARC: Delay Slot SPARC: Local / Global / In / Out Registers **SPARC:** Register Windows SPARC: Save / Restore **Spilling Registers** State v. Environment Static v. Dynamic Syntax-Directed Translation Tail Recursion Target Code Generation Three-Address Instructions / Triples / Quadruples Tiling – Rules / Patterns / Replacement / Cost Tiling (approach to code generation) Topological Sort Order Two's Complement Number Representation Unreachable Code Use-Definition (U-D) Chains Variable (or Address) Descriptors / Register Descriptors